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High Speed Optimized Adders

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Abstract

Adders are the components which are used to add two or more bits. They are mainly used in the circuits of arithmetic logic units. There are many types of adders which help have an equal range of advantages and disadvantages were among all Carry select adders contain very simple logic and less time consumption. And so here arises an idea of developing a hybrid adder using the advantages of Carry select adder, Kogge stone adder and Carry look ahead adder to speed up the arithmetic and logic operations. Carry look ahead adder is the fastest adder which reduces the delay of carry propagation. Kogge stone adder is a nonconventional adder which has the best advantage over speed computations. The idea of implementing the Hybrid Carry select adder using these two adders gives a better performance over speed, energy and power consumptions. When such a type of adder is being designed, arithmetic and logic operations can be done at a very high speed compared to other various types of adders.

Index Terms

Carry look ahead adder, Kogge stone adder, Hybrid carry select adder, Fast computations in logics, Conventional adder types.

I.Introduction

Adders are the most required component or device which are used in many electronic appliances like Microprocessors and Central processing units (CPUs). They are basic elements to perform arithmetic and logic computations. Adders are mainly used in digital systems to perform n-number of bits for arithmetic calculations. Enhancement or improvements of such systems can bring a huge development in the digital world. Hence Adders with fast computations, less power consumption and with an average requirement of area.

A vast variety of adders have been found so far. Ripple carry adder is a combination of full adders where the carry is rippled over each stage of adders. This is a time consuming process since the Ripple carry adder(RCA) takes time for carry propagation at each stage. Carry Look Ahead Adders are the adders which are the fastest over RCAs. This adder overcomes the carry propagation delay. And also it contains less number of logic gates and has been used in critical applications of time. Carry Save Adders is a kind of parallel combination of RCAs where the carry has been saved and further calculated. This is mainly useful for the multiplier logic of circuits. Since the carry is saved it makes less time consumption for operations but it is efficient only for more number bit computations. It is quite the opposite of other adders which takes time for small number of bit operations and power consuming. Carry Skip Adder is the adder which skips the carry and uses a skip logic circuit for arithmetic operations. Since 2 carry skip logic to be used in a logic which consumes power. And now comes the simple logical adder i.e., Carry Select Adder which is well known for its area requirement and speed computation characteristics.

Carry Select Adders pre-compute the possible carries and hence the delay is very less compared to the other adders. It has the structure of most arithmetic units as it decreases the propagation delay. When such adder is incorporated with Kogge stone adder and Carry look Ahead Adder a better development over adders can be implemented. Kogge Stone Adder is the adder which has better performance over time. So when a Carry Look Ahead Adder with Carry Select Adder gives a better performance over Size requirement and Carry Select Adder with Kogge Stone Adder gives a better performance over speed.Hence an Hybrid Adder can be designed with these adders which can bring a huge development in the digital world.

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II. Brief On Csla

An adder that also works as Multiplexer Comes under the category of Carry Select Adder. A Carry Select Adder is the adder that performs arithmetic values with fast computations of more intermediate values in a speedy manner.

A common conventional CSLA is a serially connected full adder which is being employed with RCA . This connection helps to add two numbers with C_{in} provided at the initial stage, the full adders that is connected will give the corresponding sum and output bits.A logic of 4-Bit RCA is given as follows

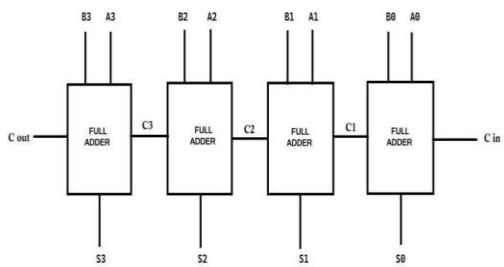


Figure-1 14 bit RCA

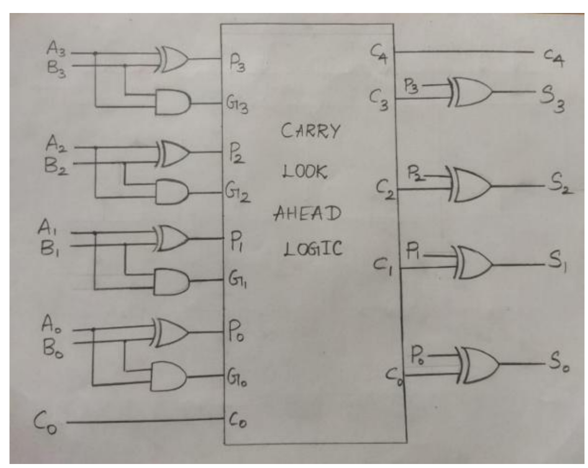
The main disadvantage of Ripple carry Adder is that the carry at each stage is to be propagated to get the output i.e., the carry ripples over the processes. This leads to increased delay of the adder. In digital circuits consisting of adders, the performance of adder speed depends on the propagation time required by the carry to proceed. The CSLA is the utmost common adder which is employed in most of the arithmetic units as it decreases propagation delay. The basic logic behind this adder is redundancy which helps in fast computation. The regular conventional CSLA consists of two RCA cells and a composed Multiplexer. In a CSLA addition of two n-bit numbers are performed by two adders hence 2-RCAs are required. First adder will consider Cin as '0' and the other adder will take Cin as '1'. After these calculations it is further processed by a multiplexer to determine the correct result.

The Carry Select Adder are of two types Uniform and Variable. In Uniform type the blocks are of identical capacity. Variable, each set is of different size which can be used to decrease the delay at input stage of carry-in. And now comes the Hybrid Adder which uses more than one adder architecture to attain higher speed. The hybrid adder is designed by considering the advantage of two adders namely Kogge Stone Adder and Carry Look Adder.

III. Carry Look Ahead Adder

This plays a vital role in the proposed adder which is used to implement in the initial stage of the proposed adder to make it spee

optimized. The drawback of RCA (carry propagation delay) is overcome by the Carry Look Ahead Adder. This fast adder calculates the carry generated by all the full adders at once increasing the complexity in the circuit. The carry is calculated earlier and then



performs addition. The carry consists of two separate parameters Carry Generate and Carry propagate. Carry propagate is denoted as P_i and Carry generate

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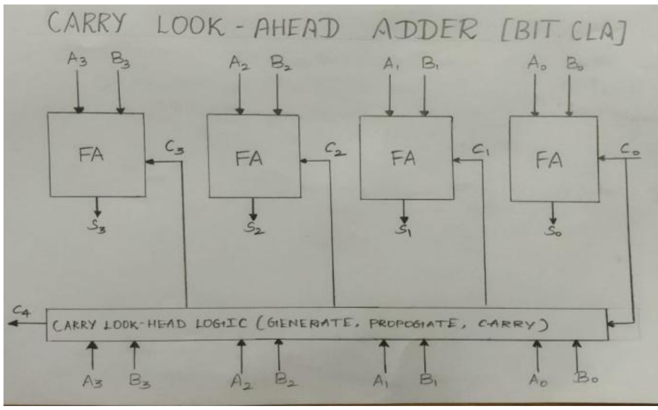
IV.The Block Diagram Of Cla:

is denoted as G_i. where i=0,1,2,…. Carry output expression becomes more complex. There is a tradeoff between area and speed.



The equations of carry-look Ahead Adder are as follows:

$$P0 = p_3 \cdot p_2 \cdot p_1 \cdot p_0$$
$$P1 = p_7 \cdot p_6 \cdot p_5 \cdot p_4$$
$$P2 = p_{11} \cdot p_{10} \cdot p_9 \cdot p_8$$
$$P3 = p_{15} \cdot p_{14} \cdot p_{13} \cdot p_{12}$$

$$G_0 = g_3 + (p_3 \cdot g_2) + (p_3 \cdot p_2 \cdot g_1) + (p_3 \cdot p_2 \cdot p_1 \cdot g_0)$$
$$G_1 = g_7 + (p_7 \cdot g_6) + (p_7 \cdot p_6 \cdot g_5) + (p_7 \cdot p_6 \cdot p_5 \cdot g_4)$$
$$G_2 = g_{11} + (p_{11} \cdot g_{10}) + (p_{11} \cdot p_{10} \cdot g_9) + (p_{11} \cdot p_{10} \cdot p_9 \cdot g_8)$$
$$G_3 = g_{15} + (p_{15} \cdot g_{14}) + (p_{15} \cdot p_{14} \cdot g_{13}) + (p_{15} \cdot p_{14} \cdot p_{13} \cdot g_{12})$$

$$C_1 = G_0 + (P_0 \cdot c_0)$$
$$C_2 = G_1 + (P_1 \cdot G_0) + (P_1 \cdot P_0 \cdot c_0)$$
$$C_3 = G_2 + (P_2 \cdot G_1) + (P_2 \cdot P_1 \cdot G_0) + (P_2 \cdot P_1 \cdot P_0 \cdot c_0)$$
$$C_4 = G_3 + (P_3 \cdot G_2) + (P_3 \cdot P_2 \cdot G_1) + (P_3 \cdot P_2 \cdot P_1 \cdot G_0) + (P_3 \cdot P_2 \cdot P_1 \cdot P_0 \cdot c_0)$$

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V.Kogge Stone Adder

KSA is commonly treated as high speed adder, which belongs to parallel prefix adders. KSAs are suitable for performing higher complex arithmetic operations and computations. The Kogge Stone Adder carry is calculated and generation of carry is done simultaneously which is possible by the increased area. This feature is really important in the electronic world and so an adaptive one. Even Though the KSAs work really fast, the area utilized is literally high. The working of KSA is interpreted by 3 stages as follow

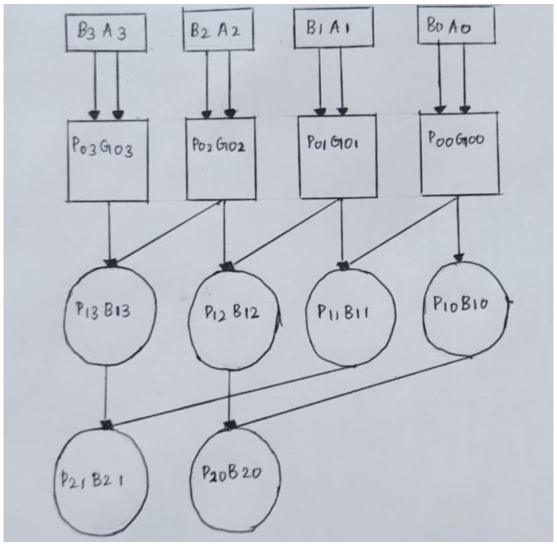

Fig.3 4-BIT KOGGE STONE ADDER

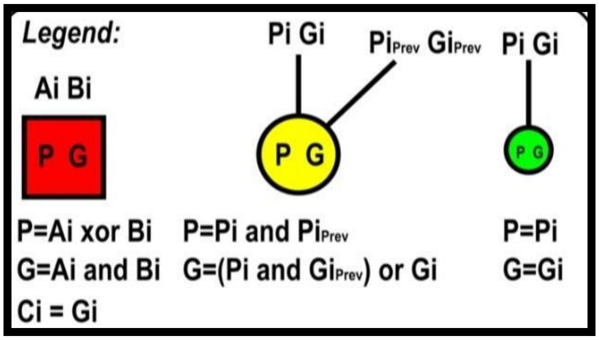

Fig.4 KSA EQUATION

VI. Hybrid Adder Csla Structure And Working

The adder is a combination of CSLA, KSA and CLA. In this design instead of 2-bit RCAs, conventional CSLAs with Kogge stone adder and Carry Look Ahead Adder is used. The main reason for employing these two adders is to optimize the delay done by other adders. Since Kogge Stone Adder is the fastest adder the carry generation is done at a speed rate. CLAs are incorporated in this modified adder to boost the efficiency of speed that provides the fast arithmetic operations.

This designed hybrid adder provided with the inputs A_i, B_i and C_{in}. A and B are the two inputs to be added. The two possible values are generated with the help of CLAs and further addition performed by the Kogge Stone Adder, corresponding output is calculated. This process takes place simultaneously.

The sum and the carry are fed into the selection unit (MUX) that selects the appropriate carry and the output is Sum and C_{out}. CLA are used in the initial positions of the adder and it becomes more complex with increased bit size, so when bit size is increased the addition process is done by kogge stone adder (KSA).The hybrid structure of CSLA is described with a block diagram of 64-bit

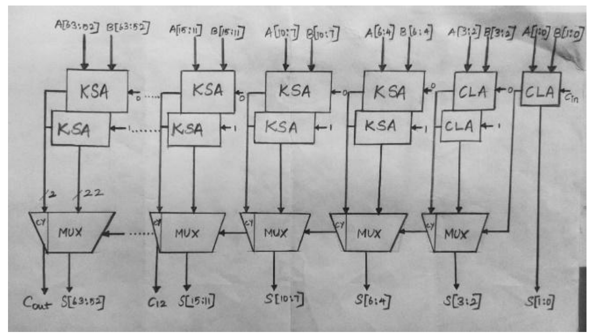

Fig.5 HYBRID 16-BIT CSLA STRUCTURE

VII. Comparison

The proposed Hybrid Adder was generated and the delay, area and power used was reduced. The whole comparison of Ripple carry adder, Carry Look Ahead Adder and also with the other adders like Carry Skip Adder, Carry Increment Adder,Carry Save Adder is also provided. The following tables show the resemblance of presented adder with other

Adders	Delay (ns)	Power dissipation (mW)	Area μm^2
RCA-Ripple carry Adder	4.208	0.206	2214
CSaA-Carry Save Adder	2.924	1.082	5904
CLA-Carry Look Ahead Adder	3.1	0.312	2160
CSkA-Carry Skip Adder	3.022	0.603	3486
CIA-Carry Increment Adder	2.90	0.261	2793
CSLA-Carry Select Adder	2.75	1.109	6201
Hybrid CSLA-Hybrid Carry Select Adder	1.76	1.44	1567

KSA-KoggeStone Adder	2.78	0.688	1181

Table No.1 Comparison of Adders

VIII.Conclusion

An efficient approach had been given to reduce the area and power dissipation of CSLA structure and development. The number of gates offers a great advantage in the reduction of area, power and delay. The replacement of RCAs in the conventional CSLA architecture with Kogge stone adder and Carry Look Ahead adder improved the speed and power consumption when there was a slight increase in area. The modified hybrid CSLA structure can be an efficient feature for VLSI Hardware implementation.

IX. References

[1] Shamim Akhter, Saurabh Chaturvedi, Kilari Pardhasardi,"CMOS Implementation of Efficient 16-Bit Square Root Carry-Select Adder" IEEE International Conference on Signal Processing and Integrated Networks, April 2015.

[2] V. Kokilavani, K. Preethi, and P.Balasubramanian "FPGA- Based Synthesis of High-Speed Hybrid Carry Select Adders"Hindawi Publishing Corporation Advances in Electronics Volume 2015.

[3]U Penchalaiah, Siva Kumar VG,"Design of High-Speed and Energy- Efficient Parallel Prefix Kogge Stone Adder", IEEE conference on system, computation, automation and networking.(ICSCA),2018.

[4] Nidhi Gaur, Anu Mehra, Pradeep Kumar." '16 Bit Power Efficient Carry Select Adder", International Conference on Signal Processing and Integrated Networks (SPIN) IEEE 2019.

[5] Gitanjali Sharma,"Study of different adders and analyze the delay ",International Journal of Advance Research in Science and Technology, Vol No.6,Issue No.01,January 2017.

[6] Nidhi Gaur, Anu Mehra, Pradeep Kumar." '16 Bit Power Efficient Carry Select Adder", International Conference on Signal Processing and Integrated Networks (SPIN) IEEE 2019.

[7] Ananthakrishnan, Anaswar Ajit, Arathi P V, Kiran Haridas, Niraj Mohan Nambiar , Devi S, FPGA Based "Performance Comparison of Different Basic Adder Topologies with Parallel Processing Adder", Proceedings of the Third International Conference on Electronics Communication and Aerospace Technology [ICECA 2019] IEEE Conference Record 45616;IEEE Xplore ISBN: 978-1-7281-0167-5

[8] Pakkiraiah Chakali, Madhu Kumar Patnala, "Design of High Speed Kogge-Stone Based Carry Select Adder", International Journal of Emerging Science and Engineering (IJESE) ISSN: 23196378, Volume-1, Issue- 4, February 2013.

[9] B.TapasviJ, K.Bala Sinduri, B. G.S.S.B.Lakshmi , N.Udaya Kumar," Implementation of 64-Bit Kogge Stone Carry Select Adder with ZFC for Efficient Area ",IEEE,2015. ,